IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods Of Enhancing Data Retention Of A Floating Gate Transistor, Methods Of Forming Floating Gate Transistors, And Floating Gate Transistors

* * * * *

INVENTORS

J. Dennis Keller
Roger R. Lee

ATTORNEY'S DOCKET NO. MI22-587

TECHNICAL FIELD

This invention relates to floating gate transistors and methods of forming the same. This invention also relates to methods of enhancing data retention of floating gate transistors.

BACKGROUND OF THE INVENTION

Floating gate transistors are utilized in some semiconductor memory cells. One type of memory cell that uses a floating gate transistor is a flash erasable and programmable read only memory (EPROM). A floating gate transistor typically includes a tunnel dielectric layer, a floating gate, an interlayer dielectric and a control gate or word line. Source/drain regions are formed operatively adjacent the floating gate and within semiconductive substrate material. A floating gate transistor can be placed in a programmed state by storing charge on the floating gate of the floating gate transistor. Typically, a large voltage, e.g. 25 volts, between the control gate and the substrate allows some electrons to cross the interlayer dielectric and charge the floating gate. The "data retention" of a floating gate transistor refers to the ability of the transistor to retain its charge over a period of time. Charge can be lost, undesirably, through electron migration from the floating gate through various adjacent materials. One problem which has confronted the industry is electron migration through the interlayer dielectric material immediately above the floating gate. The thickness of the interlayer dielectric material has an impact

on the abi of a floating gate to retain its charge. Thinner regions of the interlayer dielectric material provide undesired migration paths for electrons to leave the programmed floating gate relative to other thicker regions of the interlayer dielectric material. Hence, non-uniformity in the thickness of the interlayer dielectric material is undesirable.

A contributing factor to a non-uniformly thick interlayer dielectric material is the presence of a large number of grain boundaries at the interlayer dielectric/floating gate interface. Conductive doping of the floating gate, as is desirable, undesirably increases the number of interface grain boundaries, which in turn, increases the chances of having a non-uniformly thick interlayer dielectric.

This invention grew out of concerns associated with improving the data retention characteristics of floating gate transistors.

SUMMARY OF THE INVENTION

Floating gate transistors and methods of forming the same are described. In one implementation, a floating gate is formed over a substrate. The floating gate has an inner first portion and an outer second portion. Conductivity enhancing impurity is provided in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion. In another implementation, the floating gate is formed from a first layer of conductively doped semiconductive material and a second layer of substantially undoped semiconductive material. In another implementation, the floating gate

is formed a first material having a first average grain size and a second material having a second average grain size which is larger than the first average grain size.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a fragmentary portion of a semiconductor wafer is shown generally at 10 and comprises a semiconductive substrate 12. As used in this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Referring to Fig. 2, a layer 14 is formed over substrate 12 and constitutes a tunnel oxide layer.

Referring to Fig 3, a layer 16 is formed over substrate 12. In a preferred implementation, layer 16 constitutes a polysilicon layer which is formed to a first thickness t_1. Preferably, the polysilicon of layer 16 is undoped as formed and is subsequently doped, as through ion implantation, with conductivity enhancing impurity to a desired degree. According to one aspect, layer 16 is doped with a suitable impurity which is sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq. According to another aspect, first layer 16 is doped

with an impurity concentration which is greater than or equal to about 1 x $10^{18}cm^{-3}$. An exemplary concentration is between about 1 x $10^{18}cm^{-3}$ and 1 x $10^{20}cm^{-3}$, or greater. A suitable and preferred dopant or impurity is phosphorous. When phosphorous is utilized, the preferred sheet resistance is between about 600 ohm/sq. and 700 ohm/sq.

Alternately considered, layer 16 constitutes a first material or silicon-containing volume which is formed over the substrate and doped with a suitable impurity concentration to define a first average grain size. Accordingly, such silicon-containing volume has a first average grain boundary area per unit volume. An exemplary grain size is between about 50-100 nm, or ~~about 10~~ greater than about 25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

Referring to Fig. 4, a second layer 18 is formed over the substrate 12 and first layer 16. Preferably, layer 18 is formed directly atop layer 16 and to a second thickness t_2. Preferably, second layer 18 constitutes a material such as polysilicon or amorphous silicon which is substantially undoped relative to first layer 16. The term "substantially undoped" as used within this document will be understood to mean having an impurity concentration which is less than 1 x $10^{18}cm^{-3}$. In accordance with one aspect of the invention, second layer 18 constitutes a second material which is formed over material of layer 16 to have a second average grain size which is larger than the first average grain size of layer 16. Accordingly, second layer 18 constitutes a second

silicon-cont g volume having a second g boundary area per unit volume which is less than the first grain boundary area per unit volume. An exemplary grain size is between about 100-200 nm, or ~~greater than~~ about 25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

In a preferred implementation, the material of layers 16, 18, taken together, constitute material from which a floating gate of a floating gate transistor will be formed. Layers 16, 18 define an aggregate or combined thickness ($t_1 + t_2$). Accordingly to one aspect, the combined thickness of layers 16, 18 is less than or equal to about 1000 Angstroms. Such combined thickness can, however, range upward to around 1500 Angstroms or greater. The combined thickness can range downward as well. This is especially true as advances in scalability result in smaller floating gate dimensions. In one implementation, the first and second thicknesses are substantially the same. Accordingly, when the aggregate or combined thickness is around 1000 Angstroms, individual thicknesses t_1 and t_2 would be around 500 Angstroms. In another implementation, first and second thicknesses t_1 and t_2 can be different from one another. Accordingly, first thickness t_1 can constitute less than or equal to about 75% of the aggregate thickness. In another implementation, first thickness t_1 can constitute at least 25% of the aggregate or combined thickness of the floating gate. In yet another implementation, layer 16 can comprise between about 25-75% of the floating gate thickness. Where the aggregate thickness is

about 1000 Angstroms, the first thickness would be between 250-750 Angstroms. First thickness t_1 can be less than 550 Angstroms, or between 450 Angstroms and 550 Angstroms. In another implementation, the combined or aggregate thickness ($t_1 + t_2$) can equal around about 500 Angstroms, with thickness t_1 being equal to around 25-50 Angstroms. Other relative thickness relationships are of course possible.

Referring still to Fig. 4, layers 16 and 18 are subjected to suitable floating gate definition steps. In a first step, floating gate material 16, 18 is etched into and out of the plane of the page upon which Fig. 4 appears. Such effectively defines so-called floating gate wings which overlie field oxide which is not specifically shown in the Fig. 4 construction. The first etch partially forms a plurality of floating gates having respective inner first portions (layer 16) disposed proximate the substrate, and respective outer second portions (layer 18) disposed over the first portions.

Referring to Fig. 5, substrate 12 is subjected to suitable oxidizing conditions which are effective to form a first oxide layer 20 over second layer 18. Layer 20 constitutes a bottom oxide layer which is formed to a thickness of between about 50 Angstroms to 100 Angstroms.

Referring to Fig. 6, a layer 22 is formed over substrate 12 and preferably constitutes a nitride layer which is formed over first oxide layer 20. Substrate 12 is subsequently subjected to oxidizing conditions which are sufficient to form a second oxide layer 24 over nitride layer 22. Taken together, layers 20, 22, and 24 constitute an ONO

dielectric la which constitutes a third lay 26 of dielectric material which is formed over the second silicon-containing volume or second layer 18. Other dielectric layers are possible.

Referring to Fig. 7, a fourth layer 28 is formed over third layer 26 and comprises a conductive material. In a preferred implementation, layer 28 constitutes a third layer of polysilicon which is formed over second oxide layer 24 and will constitute a conductive line for the floating gate transistor to be formed.

Referring to Fig. 8, the various layers of Fig. 7 are etched to provide a plurality of floating gate transistors 30, 32, 34, and 36. Such defines the remaining opposing edges of the floating gates of such transistors. The floating gate transistors are also provided with respective source/drain regions which are disposed laterally proximate the floating gates. In the illustrated example, individual source regions 38, 40 and a drain region 42 are shown. Additionally, an oxide layer 44 is disposed over individual floating gates 30, 32, 34, and 36. A plug 46 comprising conductive contact film material is disposed operatively adjacent drain region 42 and serves to electrically connect with such drain region. A barrier layer 48, metal layer 50 and a passivation layer 52 are shown.

The above-described floating gate construction provides an improved floating gate transistor which is less prone to lose its charge due to electron migration from the floating gate through the dielectric layer intermediate the floating gate and the overlying word line. Such

improvements increase the data retention characteristics of the floating gate. The improvements are made possible, in part, through a more uniformly thick bottom oxide layer (oxide layer 20) of the ONO dielectric layer discussed above. Such a uniformly thick layer provides less opportunities for electrons to migrate away from the floating gate.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.